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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/623,390	07/18/2003	Peyman Hadizad	ONS00502	4626	
7590 06/17/2005			EXAMINER		
James J. Stipanuk			EVERHART, CARIDAD		
Semiconductor	Components Industries	s, L.L.C.			
Patent Adminis	stration Dept - MD/A7	ART UNIT	PAPER NUMBER		
P.O. Box 62890	-	2891			
Phoenix, AZ 85082-2890			DATE MAILED: 06/17/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)			
		10/623,390	HADIZAD, PEYMAN			
	Office Action Summary	Examiner	Art Unit			
		Caridad M. Everhart	2891			
Period fo	The MAILING DATE of this commu r Reply	nication appears on the cover she	eet with the correspondence address	;		
THE N - Exten after: - If the - If NO - Failur Any re	ORTENED STATUTORY PERIOD IN MAILING DATE OF THIS COMMUNISIONS of time may be available under the provision SIX (6) MONTHS from the mailing date of this comperiod for reply specified above is less than thirty (in period for reply is specified above, the maximum so the toreply within the set or extended period for reply received by the Office later than three months and patent term adjustment. See 37 CFR 1.704(b).	NICATION. Is of 37 CFR 1.136(a). In no event, however, imunication. (30) days, a reply within the statutory minimum statutory period will apply and will expire SIX (if y will, by statute, cause the application to become	may a reply be timely filed n of thirty (30) days will be considered timely. 6) MONTHS from the mailing date of this communione ABANDONED (35 U.S.C. § 133).	ication.		
Status						
1)⊠	Responsive to communication(s) fil	led on 28 March 2005.				
	This action is FINAL .	2b)⊠ This action is non-final.				
′=		•	matters, prosecution as to the meri	its is		
	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Dispositi	on of Claims					
4)🖂	Claim(s) 1-20 is/are pending in the	application.				
	4a) Of the above claim(s) is/s	• •	n.			
	Claim(s) is/are allowed.					
6)🖾	Claim(s) 1-4,9-12,15,19 and 20 is/a	are rejected.				
7)🖂	Claim(s) 5-8,13,14 and 16-18 is/are	e objected to.				
8)□	Claim(s) are subject to restri	ction and/or election requiremer	nt,			
Application	on Papers					
9) 🗀 -	The specification is objected to by the	ne Examiner.				
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
	Applicant may not request that any obje			,		
		• ,	awing(s) is objected to. See 37 CFR 1.1	21(d).		
		•	ached Office Action or form PTO-15	• •		
	nder 35 U.S.C. § 119	•	,			
_	_	s for forcian priority under 25 11 6	20 2 440(0) (d) 07 (6)			
a)[2. Certified copies of the priority	y documents have been received y documents have been received	i .	۵		
		onal Bureau (PCT Rule 17.2(a)).				
* S	ee the attached detailed Office action	, , , , , , , , , , , , , , , , , , , ,				
	·					
Attachment	(s)	·				
	e of References Cited (PTO-892)	4) <u>I</u> nter	view Summary (PTO-413)			
3) 🛛 Inform	e of Draftsperson's Patent Drawing Review (I nation Disclosure Statement(s) (PTO-1449 o No(s)/Mail Date <u>7-18-03</u> .		er No(s)/Mail Date ce of Informal Patent Application (PTO-152) er:	•		

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Applicant's arguments with respect to claims 1-4,9-12,15,19,20 have been considered but are most in view of the new ground(s) of rejection.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

Claims 1-4,9-12,15,19, and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Yuan, et al. (US 5,610,085) in view of Rinne, et al. (US 6,628,532B1).

Yuan, et al disclose a device which includes a FET, an inductor342, a capacitor 344, and a controller 348, which is a control circuit(col. 4, lines 44-60). In Fig. 3d there is shown a second FET 360(col. 5, lines 10-15). The FET are JFET(col. 3, lines 23-26) and the JFET are GaAs (col. 1, lines 21-26). The capacitor 344 is shown, along with the other cited devices in Fig. 3b. It can be seen that the devices are coupled to each other with the inductor coupled to a positive terminal.

Yuan, et al is silent with respect to the depletion mode FET.

Rinne, et al disclose in a dc converter that normally on FETs result in improved performance(col. 2,lines 27-39).

It would have been obvious to one of ordinary skill in the art at the time of the invention that Yuan, et al encompasses the normally on FETs as the JFETs disclosed by Yuan, et al because Yuan et al discloses that the depletion regions taught by Yuan et

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15), and the depletion region is the characteristic that results in a normally on FET as taught by Rinne, et al., as is well known in the art.

Allowable Subject Matter

Claims 5-8,13,14,16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 571-272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, B. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CARIDAD EVERYALT
PRIMARY EXAMINED

C. Everhart 6-13-05